

A compact, dual-polarized 8.51 GHz rectenna for high voltage (50 V) actuator applications

Larry W. Epp, Abdur R. Khan, Hugh K. Smith, and R. Peter Smith

Abstract-- This paper describes a dual-polarized rectenna capable of producing a 50 V output voltage for driving mechanical actuators. This work demonstrates a circuit topology that allows the output of multiple rectenna elements to be combined in series to step-up the output voltage from 18 diodes. In this work, an independent rectifying circuit is used for each of two orthogonal polarizations to minimize the rectenna size. This helps maximize the output voltage so that a 9 element array can contain 18 diodes. By proper independent combination, the output voltage is doubled over the single polarization case, producing an output combining the maximum voltage output capable from 18 individual diodes. Such panels are being explored for use on the Next Generation Space Telescope (NGST) to eliminate wiring between actuators and provide for true mechanical isolation.

Index Terms—rectenna, actuators, free space power combining and rectification

I. INTRODUCTION

A rectenna is an antenna that captures and converts RF or microwave power to DC power. It is useful as the receiving terminal of a power transmission system where DC power needs to be delivered to a load, through free space, where physical transmission lines are not feasible. It is also useful in applications where DC power needs to be distributed to a large number of load elements in an array. The power distribution is achieved by the distributed nature of microwave energy in space, eliminating the need for a large number of physical interconnects to individual load elements.

The goal of a suitable rectenna is to convert microwave energy into DC, essentially the opposite process of modern grid amplifier designs, which convert DC to microwave energy. Analogous to grid amplifiers, a rectenna can use the distributed nature of the microwave power to combine the power from many elements, which are spatially separated by the element spacing of the array or panel. Therefore the effective area of the entire rectenna

panel determines the total power an individual panel receives.

By additionally separating small individual rectenna panels across a segmented, actuator driven reflector, multiple rectenna panels can provide for power distribution without physical wiring or interconnects. If each rectenna panel is sized to provide suitable voltage to drive an actuator, this provides a spatial distribution of power to each actuator. Ideally, the individual rectenna panels on each actuator provide a source of control signals for each actuator. For example, in addition to DC power, each actuator could be remotely controlled by proper modulation of the incident microwave beam.

The development of a rectenna involves maximizing the efficiency of capturing the microwave energy by the antenna, and maximizing the efficiency of the rectification process. In this application, the rectification efficiency involves a trade-off between developing a DC power conditioning system that provides proper terminating impedance to the rectifying circuits, and generating the proper voltage needed in the particular application. The rectenna development work here was initiated as part of the development of microwave driven smart material actuators for control of Next Generation Space Telescope (NGST) by Prof. Sang Choi of NASA Langley [1]. It was desired that the rectenna panels produce an output voltage of 50 V, for minimal panel size, while operating at a frequency of 8.51 GHz.

II. ANTENNA ELEMENT DESIGN

Most previous rectenna designs have employed dipole antennas [2] – [6] and received a single linear polarization. A thin-film, printed-circuit dipole rectenna design was proposed initially by Brown [3] and had simple DC removal. This single polarization design minimized the thermal path between the diodes and the outer surface. See Fig. 1. But the printed capacitors of these thin-film designs mean they are not as readily tunable as Brown's original 'bar-type' rectenna element [3]. In practice, the 'bar-type' rectennas have been demonstrated by Dickinson in the 1975 JPL Goldstone microwave transmission demonstration to have efficiencies as high as 82.5% [7] – [8].

For dual polarization the extension of the thin film dipole design quickly encounters significant obstacles to successful implementation. A separate layer, one layer for each polarization, is required for each polarization. Electromagnetic interaction between the DC collection lines, parallel to the dipole on the orthogonal layer, can

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Larry W. Epp, Abdur R. Khan, and R. P. Smith are with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 USA.

Hugh K. Smith was with the Jet Propulsion Laboratory. He is now with Motorola, Cellular Subscriber Sector Research Laboratory, Harvard, IL 60033.

compromise the rectenna performance. Having one dipole layer "buried" beneath the other also has serious thermal problems.

In addition, the fabrication process of the dual linear dipole design can be quite challenging since diodes and chip capacitors may be potentially buried between layers of foam and/or polyimide film [6]. To avoid this, Alden and Ohno [9] developed a single foreplane design. But the dipole designs, in general, suffer from the situation that the feed circuitry and the antenna (dipole) are tightly coupled, in the sense that the twin lead transmission line impedance relates to the dipole impedance; therefore posing a constraint on the design. Also inherent with a dipole design is the fact the feed circuitry was exposed to the outside world and therefore parasitic radiation from these feed lines including harmonic radiation (generated by the diodes) could be an issue.

For dual-polarization needs, a microstrip patch design could potentially alleviate many of the problems mentioned above. The advantage of dual-polarization is two-fold: it potentially doubles the receive power per element area, and makes the rectenna capable of receiving either dual linear or a single circular polarization. The latter ability to receive circular polarization makes the rectenna panel more suitable for applications such as a circling airplane platform [2], [10].

A microstrip patch which is aperture coupled relies on an aperture, or coupling slot, to couple electromagnetic energy from a feed circuit to the microstrip patch antenna as is shown in Fig. 2. In this configuration, the antenna and the microstrip feed circuit are divorced from one another. This also allows the diode circuitry to be isolated behind the ground plane containing the coupling apertures. This ground plane, which separates the patch antenna and the feed circuit, protects the feed circuitry from the incident RF energy. As a result, the incident RF energy will not be coupled to the DC lines that collect the output power.

The ground plane also prevents the harmonics, which are generated by the diodes, from radiating back towards the incident wave. A microstrip line filter is used to prevent radiation back through the aperture feed. Due to the potential interference of generated harmonics, this concept of separating the receiving element and rectifying circuitry to prevent harmonic radiation has also been explored by other researchers [11] using a circular patch and single diode. Other researchers have explored the use of a Frequency Selective Surface [12].

A. Antenna

As shown in Fig. 2, the patch is supported above the ground plane by a lightweight foam support. This foam has a relative dielectric constant of 1.07, thereby helping to avoid any surface wave modes that may limit the microstrip patch array performance. In particular, this configuration was first discussed by Zürcher in his SSFIP (Strip Slot Foam Inverted Patch) concept in 1988 [13]. Just as important, the ground plane provides a good thermal sink for the diodes with a via connection to the ground plane. Recently, microstrip patch antennas have become

increasingly popular in rectenna development [10] – [12], [14] – [16] at 2.45 GHz and 35 GHz.

Aperture coupled microstrip patch antennas were first introduced by Pozar in 1985 [17]. In December 1986 Pozar presented a reciprocity-based method for the analysis of aperture coupled microstrip patch antennas [18]. Other researchers have offered solutions to the single aperture coupled microstrip patch antenna using modal or cavity methods [19] – [20]. More, recently, Rostan, Wiesbeck, et. al. have employed Pozar's methods in designing dual polarized aperture coupled microstrip patch antennas. These patch antennas, used for synthetic aperture radar (SAR) and satellite reception antennas [21] – [24] were the basis for the design used here.

B. Construction Details of the Aperture Coupled Microstrip Patch Antenna

The microstrip patch antennas constructed used Rohacell® 51 ($\epsilon_r = 1.07$), as the foam spacer, RT/duroid® 5880 (0.020 inches thick, $\epsilon_r = 2.2$, ½ ounce copper) as the microwave substrate, and Sheldahl's Novaclad® G2200 (50 μm thick, $\epsilon_r = 3.3$, 1 ounce copper), which is a copper clad polyimide film, on which the microstrip patch antenna was etched. Method of Moments solutions indicate that for every 0.001 inch difference in patch thickness a 10 MHz change in resonant frequency will occur.

To insure accurate thickness of the foam used, a method was developed to pre-compress the thickness of the Rohacell® to 35 mils by using a compression fixture and an oven. A piece of 40 mil thick Rohacell® foam is placed in a compression fixture which the foam is then preloaded (placed in compression). The entire assembly is then placed inside an oven that is heated above 375° F, the temperature at which the Rohacell® loses its compressive strength. Using 35 mil shims sets the final thickness.

Typical solder reflow temperatures are above 400° F and the Rohacell® begins to expand at 375° F. Therefore, if the Rohacell® is bonded to the RT/duroid® prior to the solder reflow process and then exposed to the solder reflow, the foam severely distorts, destroying the rectenna panel. An alternative is to use a room temperature vulcanizing silicone rubber adhesive, such as Dow Corning® 3140 RTV. Using the 3140 RTV Coating allows for components to be wave soldered to the RT/duroid®, then the RT/duroid® can be bonded to the Rohacell foam. The actual fabrication process uses a Maher bar (grooved bar) to apply a uniform coat of adhesive; thereby insuring repeatability in the fabrication process.

C. TRL Standards for Patch Measurement

The input impedance of the microstrip patch antennas was measured on a HP8510C network analyzer using a TRL (through-reflect-line) calibration procedure [25]. The HP8510C is first calibrated with the TRL standard, after which, both ports of the antenna test fixture are connected to the network analyzer. The TRL calibration

accounts for the loss of the 3.81 cm (1.5 in.) of microstrip line and SMA connector feeding the aperture. Similar calibration standards will be used to determine the line and connector loss in the effective area measurements that follow.

D. Patch Measurement

The goal of the microstrip patch design is to present a low return loss (S_{11} , S_{22}) at 8.51 GHz. It is also desired to have isolation between the two ports (a low S_{21} , S_{12}) of Fig. 2. The scattering parameter data and final patch dimensions are shown in Fig. 3. The measured return loss in Fig. 3 is shown to exceed 18 dB (only port one is shown due to symmetry) at 8.51 GHz.

The measured resonance frequency, for optimum return loss, was 8.565 GHz. The simulations indicate a worst case coupling between the two ports greater than -20 dB, while actual measurements were slightly greater than this value. Measurements gave a worst case coupling between ports of -18.5 dB (at 8.07 GHz) for all frequencies below 10 GHz. To correct for the foam compression, the relative permittivity was increased by the ratio of compressed to uncompressed height to $\epsilon_r = 1.2$.

Fig. 3 also shows the predicted gain and scattering parameters up to 18 GHz. This allows the simulated parameters to be shown at the first harmonic of the operating frequency at 17.02 GHz. The measured results stop at 16 GHz where the microstrip line becomes overmoded. (Note the increase in measurement error for S_{11} , as compared to the predicted value, at 16 GHz.) The predicted patch gain at 8.51 GHz is 8.4 dB. At the first harmonic frequency the gain is less than -17 dB, indicating that the harmonic radiation is not radiated back through the coupling aperture and towards the signal source. The additional low pass filter, discussed below, provides further suppression of unwanted harmonic radiation.

III. DIODE MEASUREMENT AND MODELLING

A. Diode Background

Most rectenna designs have followed Brown in using a single diode in a clamping circuit configuration rather than a traditional multiple-diode rectifying circuit. At microwave frequencies, these rectenna circuits are highly nonlinear and difficult to design based upon purely analytic equations. Commercially available harmonic balance simulators are useful, but necessarily limited by the accuracy of the diode model at large signal. Therefore previous works that have developed equivalent circuits of the diode have also validated with experimental results [4, 12, 26].

Since optimally tuning a rectifier requires ideal tuning at harmonics as well as the fundamental tone, parameters of any diode model must be known at the harmonics as well. Experimental large signal measurements provide a method of extracting and verifying diode models and of searching for maximum efficiency. Since the tuning done here is purely empirical, there is no guarantee that the

results actually represent the best that could be achieved with a given device. However, the inverse is true - a properly designed microstrip circuit, especially with extra components (e.g., chip caps, etc.) should certainly do as well as the empirically tuned results presented here. It was also found that optimization of efficiency using non-linear simulations was time consuming, and of course inaccurate until diode models were extracted.

B. Diode Measurement

For the purposes of this effort diodes readily available in a packaged format with large breakdown were chosen. The diode used is the commercially available M/A-Com 40401 Schottky diode in package model 213. For the purposes here the rectification efficiency is defined to be $(P_{DC}/(P_{inc}-P_{ref}))$, where P_{DC} is the DC output power, P_{inc} is the incident RF power, and P_{ref} is the reflected RF power). Overall efficiency is defined by (P_{DC}/P_{inc}) .

The DUT (device under test) in Fig. 4 consists of a microstrip test fixture with the diode connected in a shunt-to-ground configuration. The DUT could more specifically be considered to be the diode on the fixture. The test fixture included a ground via next to the diode location. All power measurements were made by manually tuning the input and output microstrip lines with small gold-coated silicon chips in an effort to provide suitable harmonic terminations. In addition a Maury microwave tuner at the output contributed to tuning as well as blocking the RF signal.

Measurement results at the design frequency of 8.51 GHz indicated a maximum overall efficiency of 66% with 65 mW of DC output power, and over 100 mW DC output power for a lower efficiency of 62%. This diode was found to exhibit a higher output voltage and higher efficiency than a similar diode by another manufacturer. Note that by choosing commercially available diodes, these diodes were not optimized for maximum efficiency in this application, and therefore higher efficiencies are certainly possible. The output voltage increased from 3.2 V to 4.1 V at the lower efficiency of 62%, indicative of the trade-off between maximum output voltage and efficiency expected. The large output voltage of 4.1V would allow for maximum output voltage if a suitable combination method could be found.

C. Diode Model

The diode is the most critical component in the rectenna element. All aspects of performance of the rectenna depend primarily on the diode parameters. The series resistance, for example, directly limits efficiency through I^2R loss. The junction capacitance, together with package capacitance and lead inductance, affects how harmonic currents oscillate through the diode. The breakdown voltage limits the power handling capability of each rectifying circuit. These parameters also affect the match of the circuit. Since the diode, as a power-rectifying element, must operate in a large signal environment, the diode model needs to be valid for a wide range of biasing. Finally, since high efficiency requires a large amount of

harmonics to be produced, the model also needs to be valid over a wide frequency range.

The diode model used for patch rectenna element simulations is shown in Fig. 5. The capacitor and the inductor were added as the package capacitance and lead inductance. Values for diode parameters such as grading coefficient (M), transit time (TT), energy gap (EG), and saturation-current temperature exponent (XTI) were chosen to simulate a Schottky diode. Other parameters, such as saturation current (IS), series resistance (RS), junction capacitance (CJO), and current at breakdown voltage (IBV) were chosen so that the DC performance of the model agreed with measured data.

The simulation data for the DC performance is shown in Fig. 6. The voltage, current, and resistance data were taken from the IV curve, and the total capacitance was measured by resonating the diode with a series inductor. As can be seen, the simulation data agrees well with the measured data shown in Fig. 7. The breakdown voltage was selected to be slightly higher since it was possible to select diodes, with breakdown around 9.5V, for use.

IV. RECTENNA CIRCUIT DESIGN

A. Circuit Design

The patch rectenna is most easily implemented using standard microstrip lines. Fig. 5 shows the basic rectenna circuit topology. In order to economize the use of real estate, an attempt was made to use a minimum number of stubs for the input filter/matching section. The line lengths were also made as short as possible in order to minimize the RF losses. The corresponding microstrip implementation of V_{pol} and H_{pol} circuits, for each of the two patch apertures, is shown in Fig. 8. Note the stepped line impedance and chip capacitor performs the final steps of low pass filtering and matching. The circuits were optimized for an incident power of 100mW, the expected reflection is 3 to 4 mW, and the expected overall efficiency was 65%.

B. Measurement of Unit Cells

Measurements of the unit cells show in Fig. 8 were first completed without the microstrip patch. Fig. 4 shows the test setup used to test the unit cells. The HP8671B frequency generator and the Hughes TWTA provided the incident power. Both the incident and reflected power were simultaneously monitored using the Narda 10dB couplers and the HP438 power meter. A short section of waveguide served as a DC block in the coaxial lines to prevent any DC loading on the input port of the DUT. The DUT consisted of a single unit cell with a circuit for H_{pol} and a circuit for V_{pol} in the same layout, as they would appear in an array. The input microstrip lines, however, were extended to the edge of the substrate to coaxial connectors. DC output was picked off the circuit by simply soldering a single-strand wire directly to the DC bus line. A decade box was used as the load.

Initial measurements showed that, in particular, the reflected power from the rectifying circuitry was much

higher than expected, approximately 50%. This difference was due to a discrepancy between the placement of the via holes in the circuit schematic and the physical layout. The movement of the via holes turned out to be significant.

With minimal movement of existing components, and therefore minimal board re-design, simulation and measurement showed that additional tuning stubs could reduce the unwanted reflections. The trade-off was that the expected overall efficiency was expected to fall to 60%. Fig. 8 shows the unit cell with the additional tuning stubs, show shaded, referred to here as Prototype 2.

C. Analysis and Measurement Comparisons

Several unit cells of this version (Prototype 2) were fabricated and measured. Figs. 9 and 10 show the measured results for 3 separate boards. Note that the rectification efficiency of all circuits remained close to the design overall efficiency of 60%, with high overall efficiency when reflected power was minimized. The average output voltage of the H_{pol} circuits was 4.14 V at an average overall efficiency of 57.7% when using a load resistance of 325 Ω . This desirable result meets the maximum output voltage from the diode measurements.

The average output voltage of the V_{pol} circuits was lower, 3.84 V, at an average efficiency of 49.8% with a load resistance of 325 Ω . The trade-off of the higher output voltage for efficiency is indicated by the lower average output voltage of 3.56 V for the higher average efficiency, 53.7%, when a load of 250 Ω is used. Higher sensitivity to variations in component assembly may have contributed to the lower average overall efficiency for the V_{pol} circuits. The fact that V_{pol} circuit of board 2 performed as well as the H_{pol} circuit of board 2 indicates this to be due to variations in component assembly.

V. PANEL MEASUREMENT

A. Rectenna panel: 3 by 3 elements

Rectenna panels consisting of a 3 by 3 arrangement of unit cells were fabricated using the Prototype 2 circuitry. The average output voltage of the circuits was 4 V, requiring the series connection of 13 circuits to reach the design goal of 50 V. Since each patch provides two circuits, one for V_{pol} and one for H_{pol} , the minimum number of cells required is 7 patch elements. Choosing the minimal square array containing at least 7 patches leads to an array of 3 elements by 3 elements, for 9 total patch elements.

The effective area of a single patch element is given by,

$$A_p = G_p \frac{\lambda^2}{4\pi} \quad (1)$$

Where G_p is the gain of the patch, or 8.4 dB at 8.51 GHz. The effective area for a single patch, before placement in the array, is therefore 6.8 cm². In order for the array to absorb all the incident power, it is necessary that the unit cell area be less than 6.8 cm². For rectangular spacing, a

minimal cell-to-cell spacing of 2.62 cm is then required. Accordingly, a more dense cell-to-cell spacing of 1.97 cm was chosen to further shrink the overall panel size while still leaving sufficient room for the panel circuitry.

B. Calibration of Measurement Chamber

In order to ensure that the rectenna panel could be efficiently measured in the far field, a custom-built measurement chamber was designed to allow quick access to the panel. Fig. 11 shows the measurement chamber with the rectenna panel holder above the transmit horn. The standard gain horn used to illuminate the rectenna is a Narda 640 Standard Gain Horn. The gain of the Narda 640 @ 8.51 GHz (frequency of the incident microwave energy) is 15.1 dB. Fig. 12 shows the front side of the rectenna panel in the chamber.

The Friis transmission equation is employed to verify the power density on the plane containing the rectenna. An identical Narda 640 standard gain horn is used as the receive horn at the location of the rectenna panel. To calculate the power received by this receive horn the Friis transmission equation is used and the system calibration is checked and measurement chamber accuracy verified. The measured gain of the standard gain horn is 15.03 dB, for an error of 0.07 dB.

C. Effective Area Measurement of the 9 Array Elements

During the diode and unit cell measurements, the overall efficiency was defined to be the total DC output power at the load in proportion to the incident power. Thus any power that is reflected by the circuitry is not converted into DC power and decreases the overall efficiency. Likewise in the panel measurement, overall efficiency should be defined such that any reflected power from the panel lowers the overall efficiency. An over-simplified and erroneous method of computing overall efficiency for a rectenna panel is to use the power density striking the rectenna panel from the Friis transmission equation multiplied by the physical panel surface area to compute the "received" power.

But more correctly the received power is given by,

$$P_{\text{recv}} = \frac{P_{\text{trans}} G_{\text{trans}} A^{\text{eff}}}{4\pi R^2} \quad (2)$$

where A^{eff} represents the maximum effective area of the panel as the sum of the maximum effective area of each patch in the array configuration. Thus it can be seen that for rectenna panel applications it is desirable, and possible, for the maximum effective area of the panel to exceed the physical area of the panel. And, that the maximum effective area of each patch must be measured in the array configuration under matched conditions, i.e. with no reflection, when mutual coupling is present.

If the overall panel efficiency is then defined as,

$$\eta_o = \frac{P_{\text{DC}}}{P_{\text{recv}}} = \frac{4\pi R^2 P_{\text{DC}}}{P_{\text{trans}} G_{\text{trans}} A^{\text{eff}}} \quad (3)$$

any power reflected from the rectenna panel will be provide a decrease in the overall efficiency.

To properly compute the maximum effective area of each patch in the array configuration, a rectenna panel was built where a microstrip line leading to a SMA connector replaced each rectenna circuitry as shown in Fig. 13. Each port was individually tuned until the return loss for all patches exceeded 21 dB with all other ports matched. By symmetry, only one polarization was measured and the panel rotated for the orthogonal polarization. The line losses and connector losses were removed by calibration standards, as discussed previously, for each of the two microstrip feed line configurations. To ensure accuracy of the effective area measurements for the tightly packed array, the coupling between ports was measured and found to be less than 17.5 dB for all ports. This low mutual coupling for this densely packed array can be primarily contributed to the use of the low dielectric foam superstrate.

The results of the effective area measurements are shown in Fig. 13. The transmitted polarization was a single linear polarization at an angle of 45 degrees, in order to excite both patch ports equally. The effective area was averaged between the two orthogonal ports of each patch. Note that the effective area of the center patch closely matches the physical unit cell area, as expected. Note also that the effective area of the corner patches is slightly larger than the unit cell area, since these patches are on the outside of the array.

In order to minimize the measurement discrepancies in the panel measurements that follow, the corner and center-edge effective area measurements were averaged using a symmetry argument. The total effective area of the 3 by 3 panel was then found to be 1 cm more than the physical area of the panel, or 3% greater than the physical area. Data from Port 8 was thrown out, since due to symmetry conditions it was evident that the proximity of the SMA connector from Port 5 was effecting the measurement.

D. Panel Results

To maximize the output voltage of the panel, a series combination of all individual rectenna circuits was desired. To make this possible, the ground plane (which contains the coupling apertures) around each individual patch was DC isolated below each patch. To ensure RF connection, a thin layer of copper-coated polyimide was used to ensure capacitive coupling. Opposing installation of the diodes for each of the patches orthogonal ports correctly, see Fig. 14, allowed for a series output voltage for each patch. It was found that in order to properly reverse bias all diodes when power is applied that additional resistance between the isolated ground planes was desirable. And the additional resistance allowed each isolated ground plane to discharge when power was removed, protecting the diodes.

Fig. 15 shows the measured results of the rectenna panel when loaded for optimum overall efficiency with a load resistance of 5400 Ω . The overall efficiency is calculated via (3). The load resistance of the entire panel is, in general, 18 times the unit cell resistance. The series connection of the circuits on the panel involved connecting

slightly different, not identical, circuits. Therefore a starting load resistance of approximately 18 times $325\ \Omega$ or $5850\ \Omega$ was indeed close to giving optimal overall panel efficiency.

The overall panel efficiency exceeds 52% over a large region of input powers, with a peak of 53% at a receive power of $38.8\ \text{mW/cm}^2$. It also shows that the desired output voltage of 50 V can be achieved for an input power density of $25.2\ \text{mW/cm}^2$. For the Narda 640 standard gain horn, this requires a transmit power of 13.6 W at a distance of 37.1 cm to provide 50 V of output power. Note that to provide maximum efficiency, the panel requires not only sufficient loading, but sufficient input power to place the diodes in an efficient region of operation. The peak overall panel efficiency is 4% less than the average efficiency of the H_{pol} unit cell measurements and 1% less than the average V_{pol} unit cell efficiency (measured without the patch via microstrip line). This indicates that additional gains in efficiency are likely from further optimization of the unit cell.

Fig. 16 shows the final configuration for this application. By increasing the load resistance, the required 50 V output could be obtained for a low incident power density of $6.3\ \text{mW/cm}^2$. This corresponds to only 3.4 W of transmit power at a distance of 37.1 cm.

Since the expected output voltage of 18 diodes in series could exceed the desired output voltage, a method of producing more than one 50 V output was desired. By attaching commercially available boost regulator circuits it was possible to obtain two 50 V outputs. The series output of 5 patches, or 10 circuits, was used to drive one regulator and the remainder to drive the additional regulator. Fig. 17 shows typical output when the boost regulator circuits were driving the large impedance of a voltmeter. Although interesting, this capability has not yet been tested for suitability when driving actuators that will present a lower impedance.

VI. CONCLUSIONS

A compact rectenna capable of producing a 50 V output suitable for driving mechanical activators has been demonstrated. The advantage of the aperture coupled rectenna configuration over previous dipole rectenna designs: it is more amenable to dual polarization incidence and more suitable to series combination of outputs.

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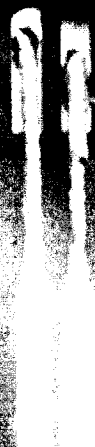
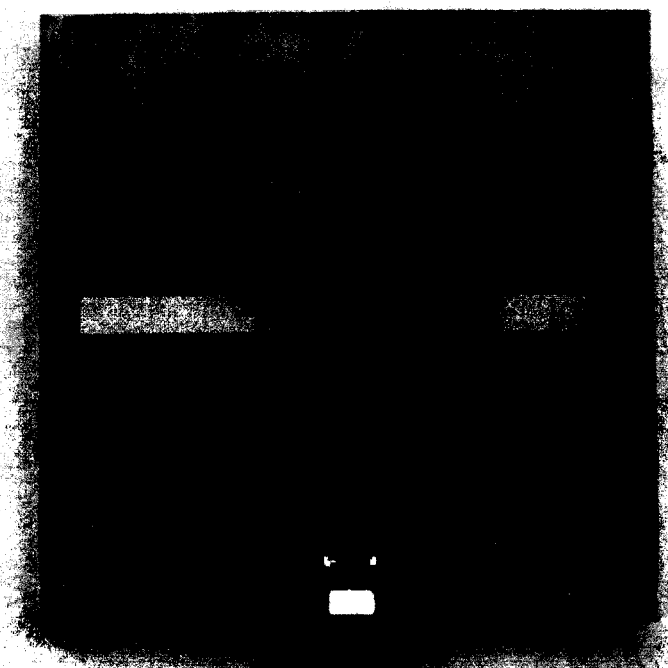
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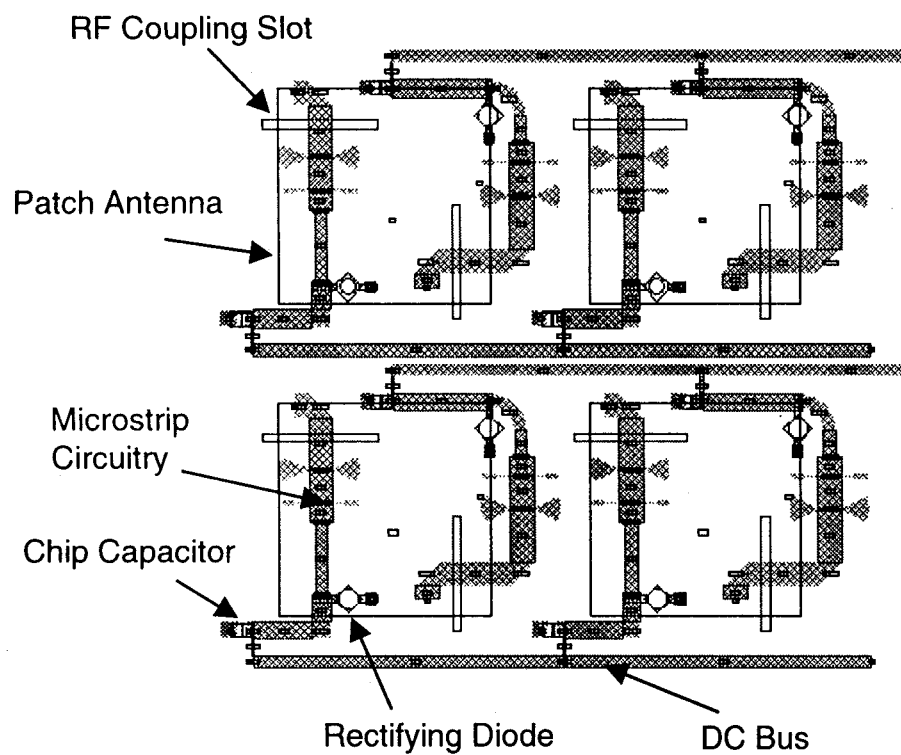
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Fig. 1. Basic thin film dipole design for a single polarization. This picture shows a single cell used for waveguide simulation.



Microstrip Circuitry



Panel Construction

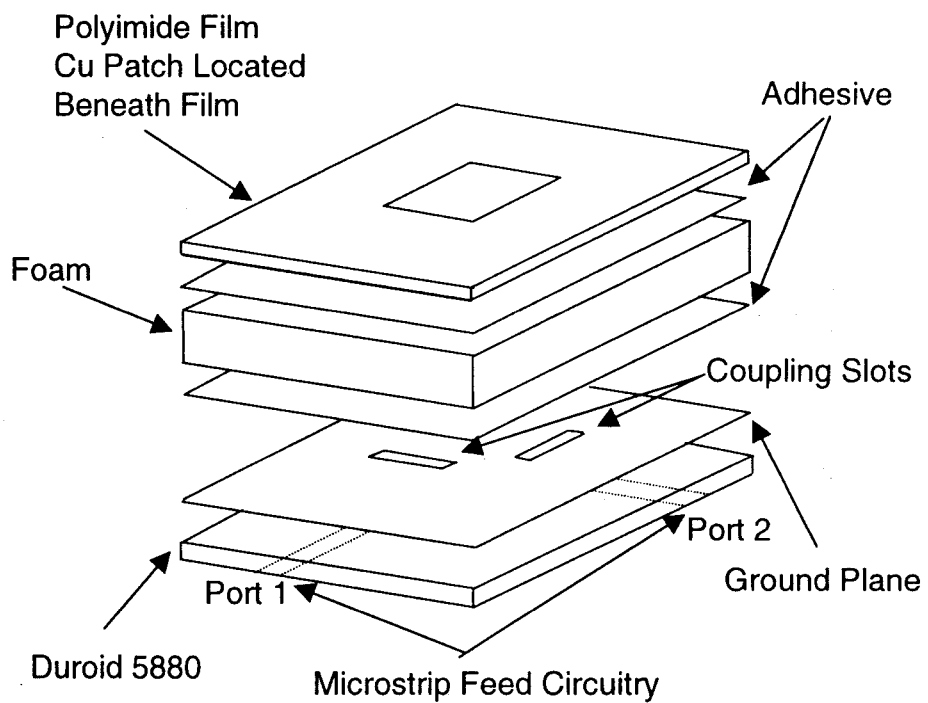


Fig. 2. Foam supported dual-polarized aperture coupled patch rectenna.

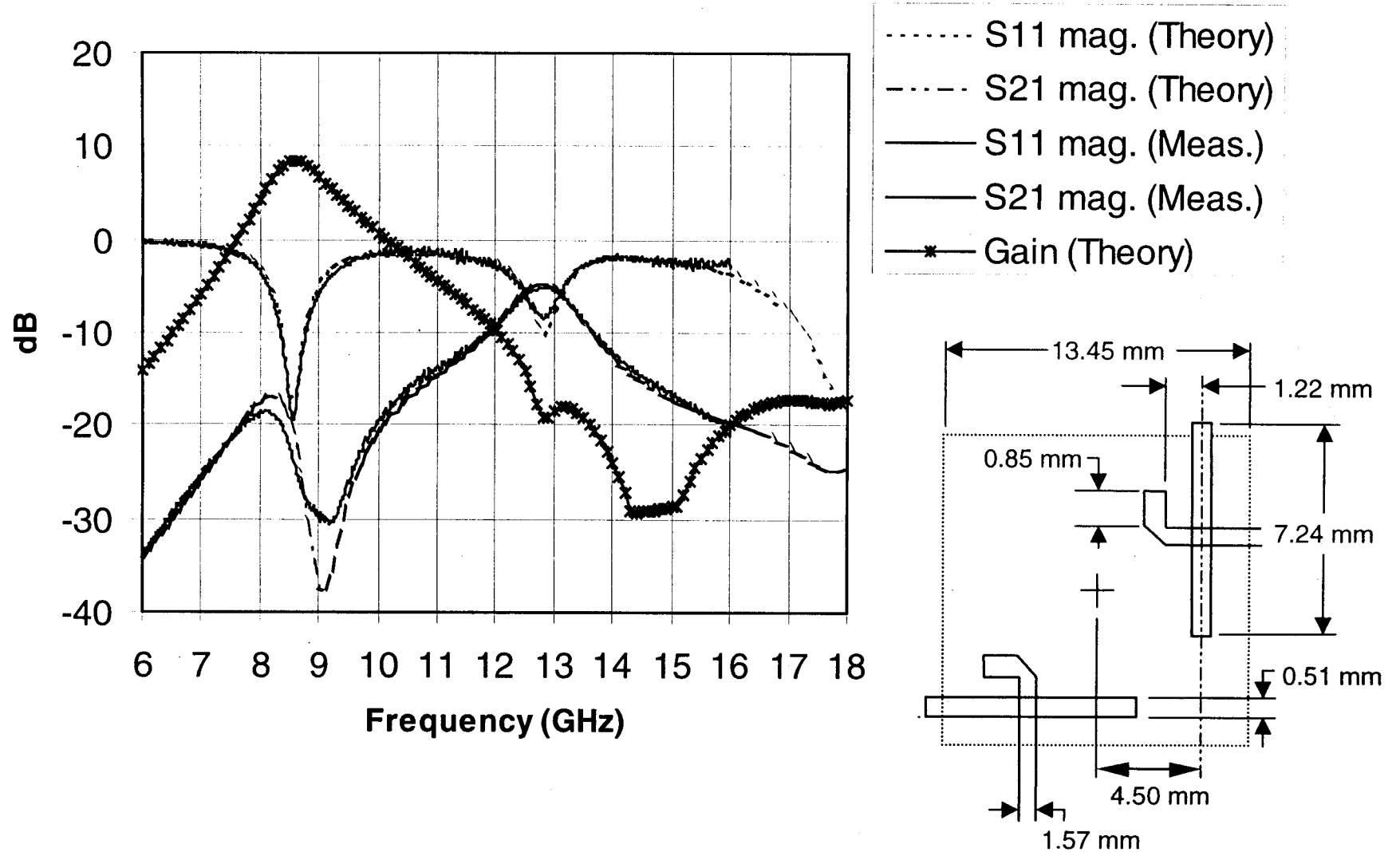


Fig. 3. Comparison of theoretical and measured values for the S parameters of the dual polarized patch. Final patch dimensions as given. The calculated results are shown over the entire frequency range, the measurements end at 16 GHz.

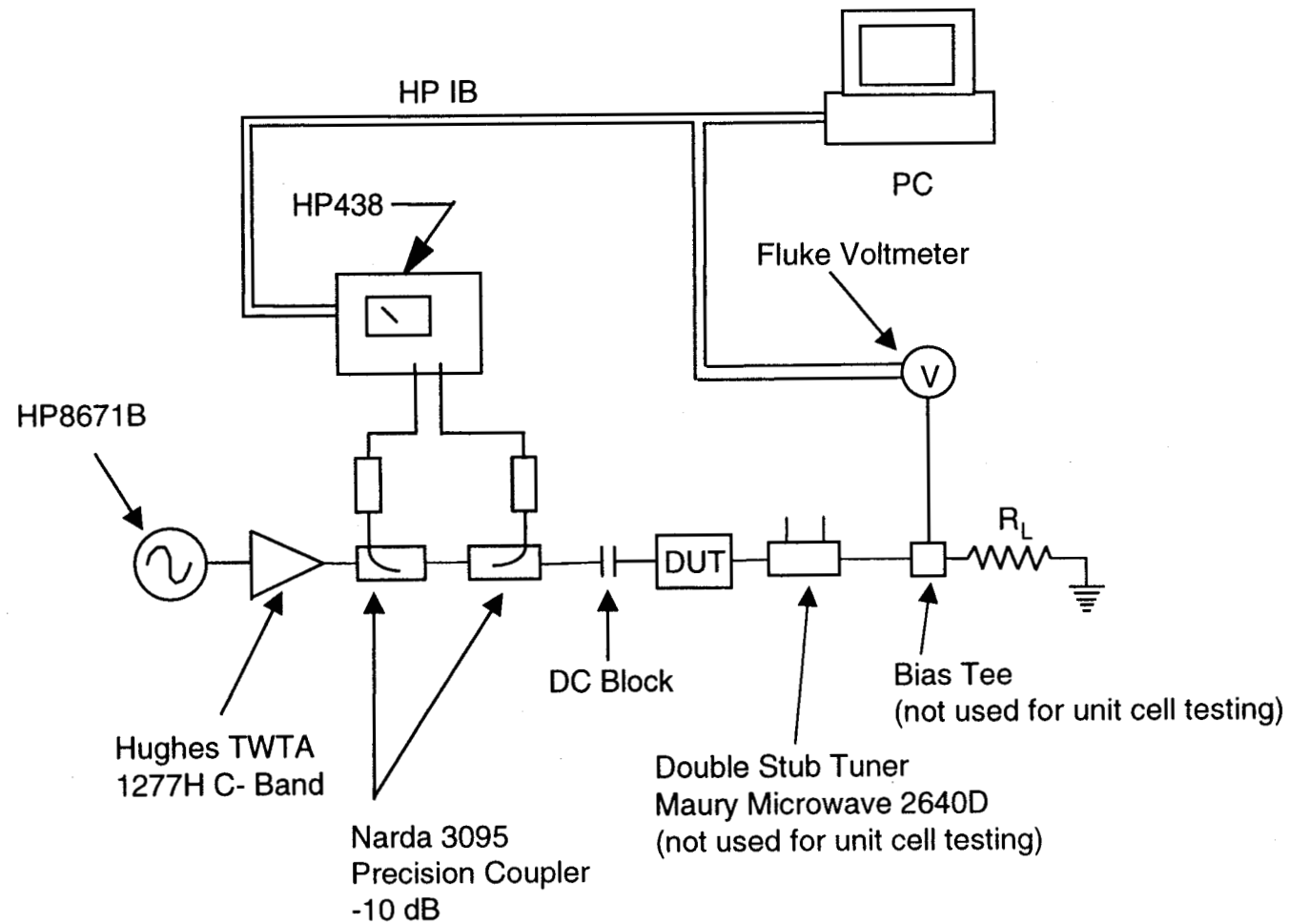
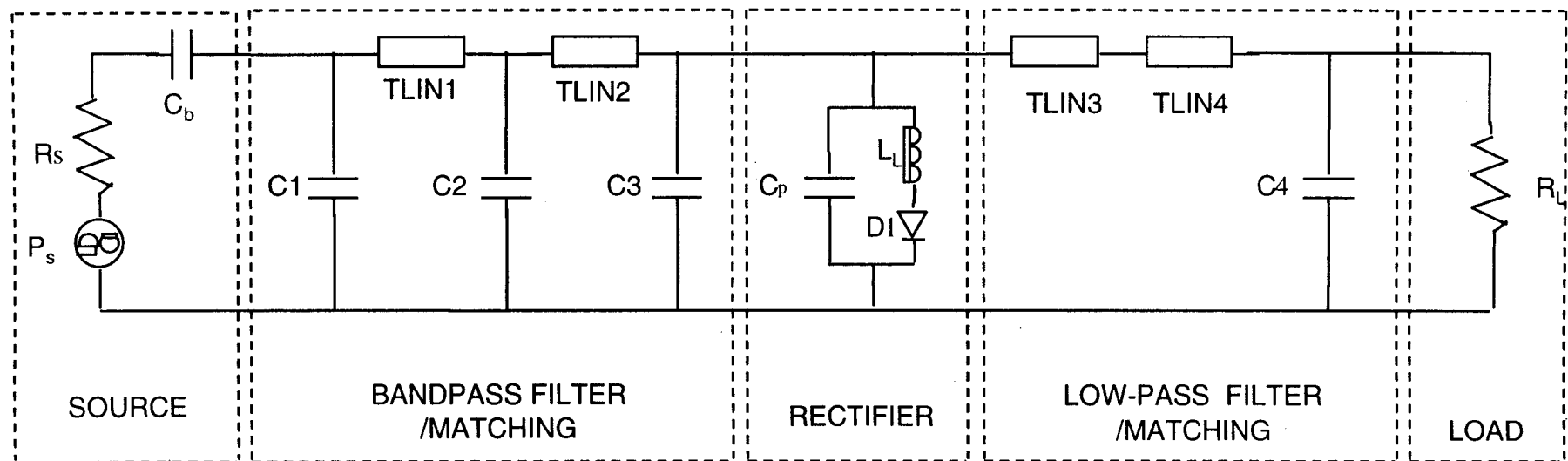


Fig. 4. General test setup used for diode and unit cell measurements.



RF Power

DC Power

Diode model: MA_COM	EG = 0.8	IKF = 0
IS = 2.46e-11	XTI = 2	NBV = 1
RS = 6.5	KF = 0	IBVL = 0
N = 1.55	AF = 1	NBVL = 1
TT = 0	FC = 0.5	TBV1 = 0
CJ0 = 1.0e-13	BV = 9.5	TNOM = 27
VJ = 0.6	IBV = 7.57e-9	FFE = 1
M = 0.5	ISR = 0	
	NR = 2	

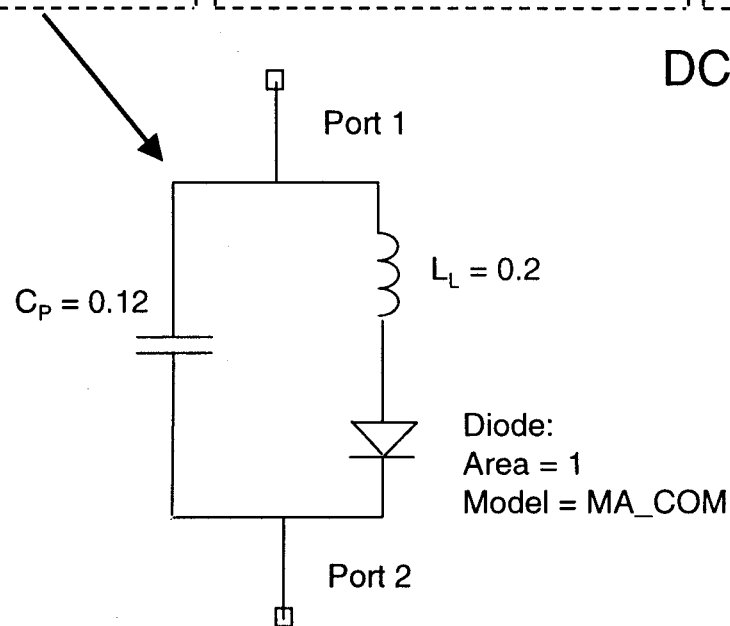


Fig. 5. Basic rectenna element circuit topology and diode model used in simulation of patch rectenna element.

	Vf1 (V)	Vf2 (V)	Vf3 (V)	Ir1 (A)	Ct (pF)	Vb (V)	Rs1 (Ω)	Rs2 (Ω)
Stimulus	.01mA	.10mA	1.0mA	1.0V	0.0V	.01mA	4.5-5.5mA	9.5-10.5mA
Model	.517	.611	.710	3.0E-11	.229	9.6	15.5	11.5

Fig. 6. Simulation data for M/A-Com 40401 Schottky diodes.

	Vf1 (V)	Vf2 (V)	Vf3 (V)	Ir1 (A)	Ct (pF)	Vb (V)	Rs1 (Ω)	Rs2 (Ω)
Stimulus	.01mA	.10mA	1.0mA	1.0V	0.0V	.01mA	4.5-5.5mA	9.5-10.5mA
Diode#1	.566	.635	.714	2.8E-11	.264	8.18	15.2	11.2
Diode#2	.570	.541	.726	7.5E-11	.228	9.36	20.8	13.6
Diode#3	.549	.618	.698	4.5E-11	.267	7.55	14.4	11.2
Diode#4	.556	.626	.706	3.1E-11	.204	7.97	15.6	9.2
Diode#5	.568	.636	.718	3.5E-11	.266	8.28	15.6	12.0

Fig. 7. Measured data for M/A-Com 40401 Schottky diodes.

Unit-Cell of 3 by 3 Rectenna

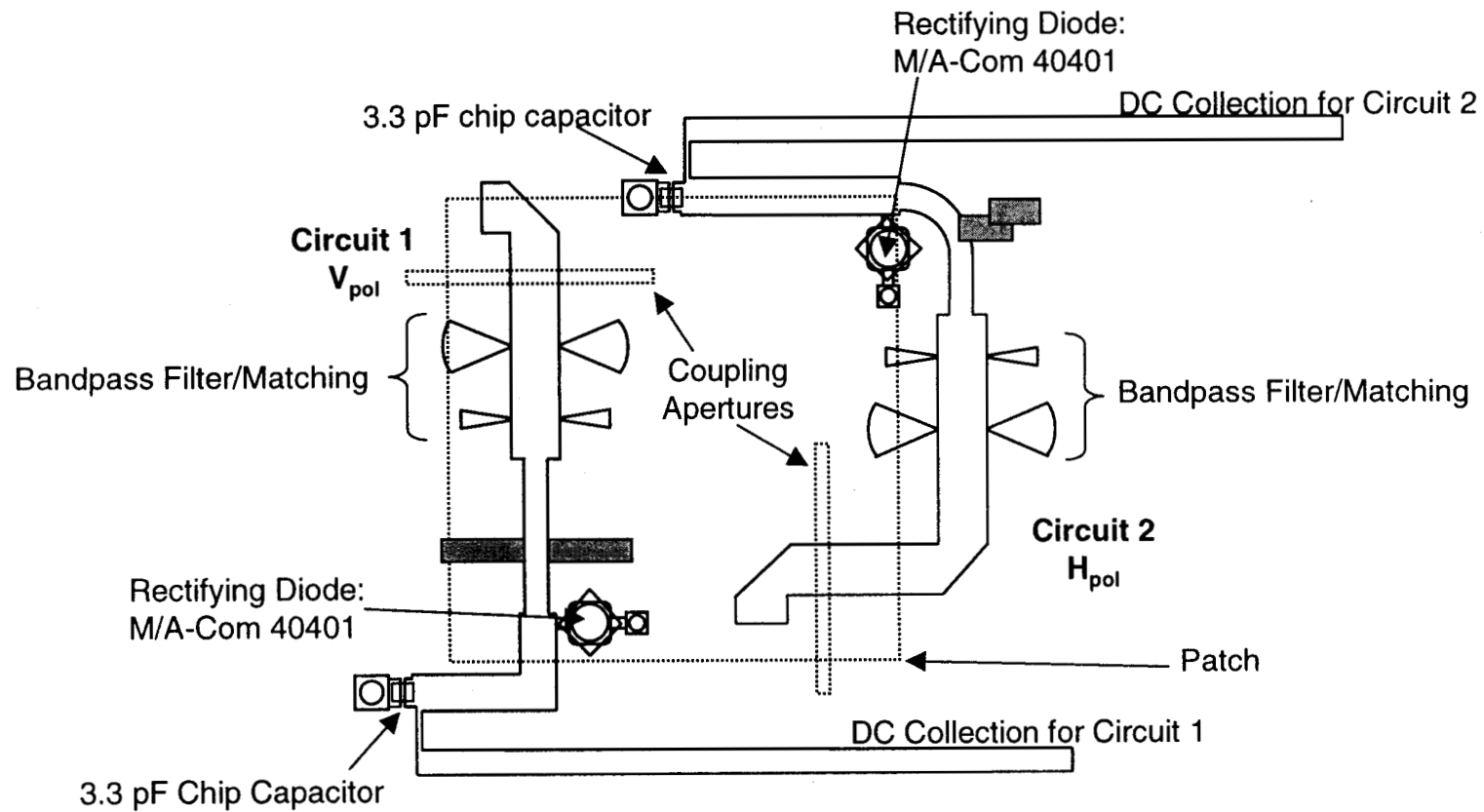


Fig. 8. Dual polarized rectenna: rectifying circuitry showing details of circuits for the two polarizations.

Frequency, GHz	Board #	Incident Power, W	Reflected Power, W	Load Resistance, Ω	DC Output Voltage	Rectification Efficiency	Overall Efficiency
8.51	1	0.106	0.024	250	3.49	59.6	45.9
8.51	1	0.086	0.026	325	3.36	58.3	40.6
8.51	2	0.094	0.000	250	3.81	62.0	61.8
8.51	2	0.090	0.002	325	4.23	62.2	61.1
8.51	3	0.086	0.013	250	3.39	63.2	53.5
8.54	3	0.100	0.021	325	3.93	60.5	47.8

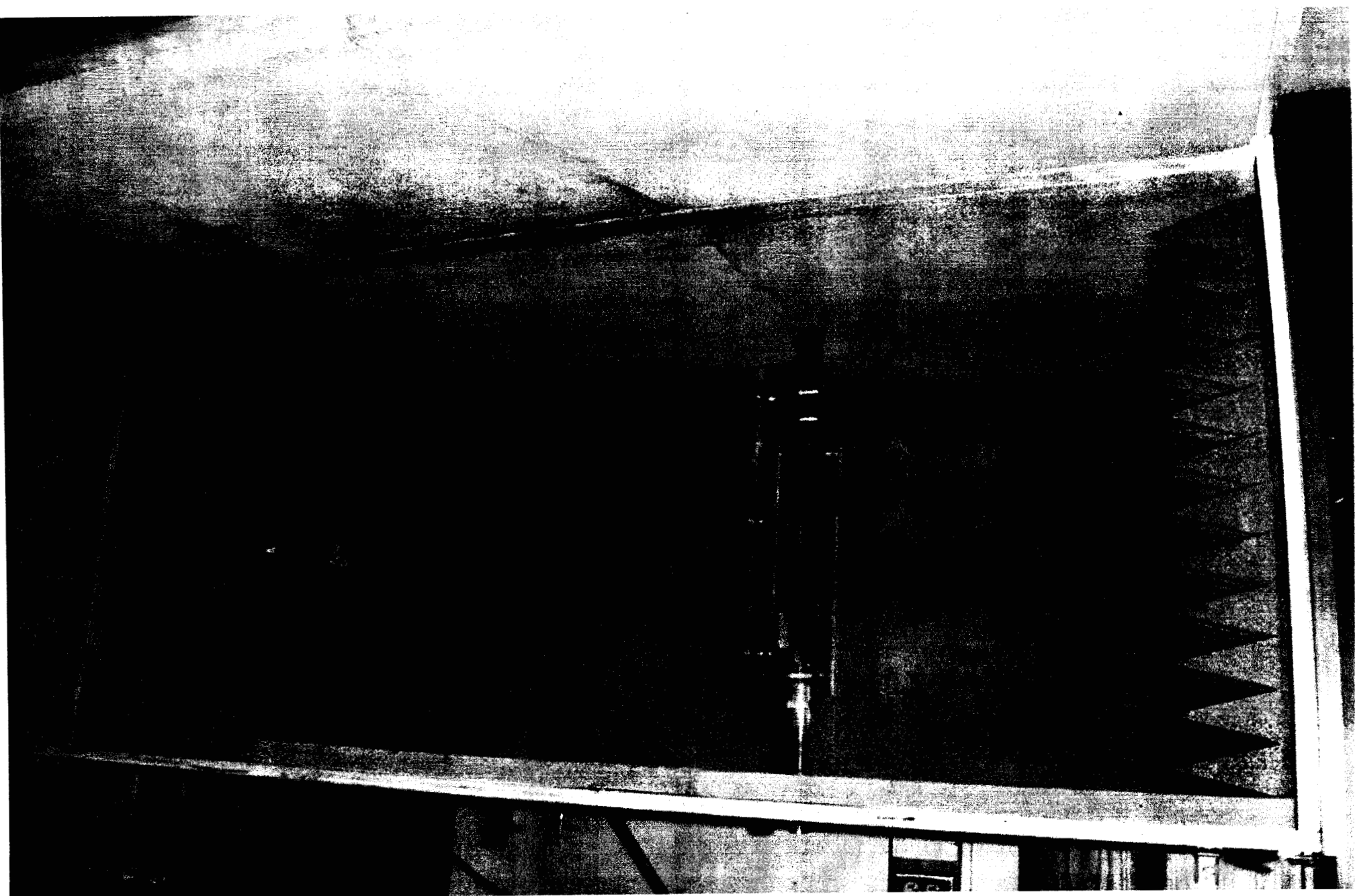
Fig. 9. Typical unit cell results from prototype 2 for V_{pol} circuit.

Frequency, GHz	Board #	Incident Power, W	Reflected Power, W	Load Resistance, Ω	DC Output Voltage	Rectification Efficiency	Overall Efficiency
8.51	1	0.104	0.001	250	4.01	62.5	62.1
8.51	1	0.100	0.000	325	4.42	60.1	60.1
8.51	2	0.098	0.002	250	3.8	60.1	58.9
8.51	2	0.091	0.000	325	4.17	59.2	59.0
8.51	3	0.086	0.004	250	3.53	61.3	58.1
8.51	3	0.078	0.009	350	3.84	61.1	54.0

Fig. 10. Typical unit cell results from prototype 2 for H_{pol} circuit.

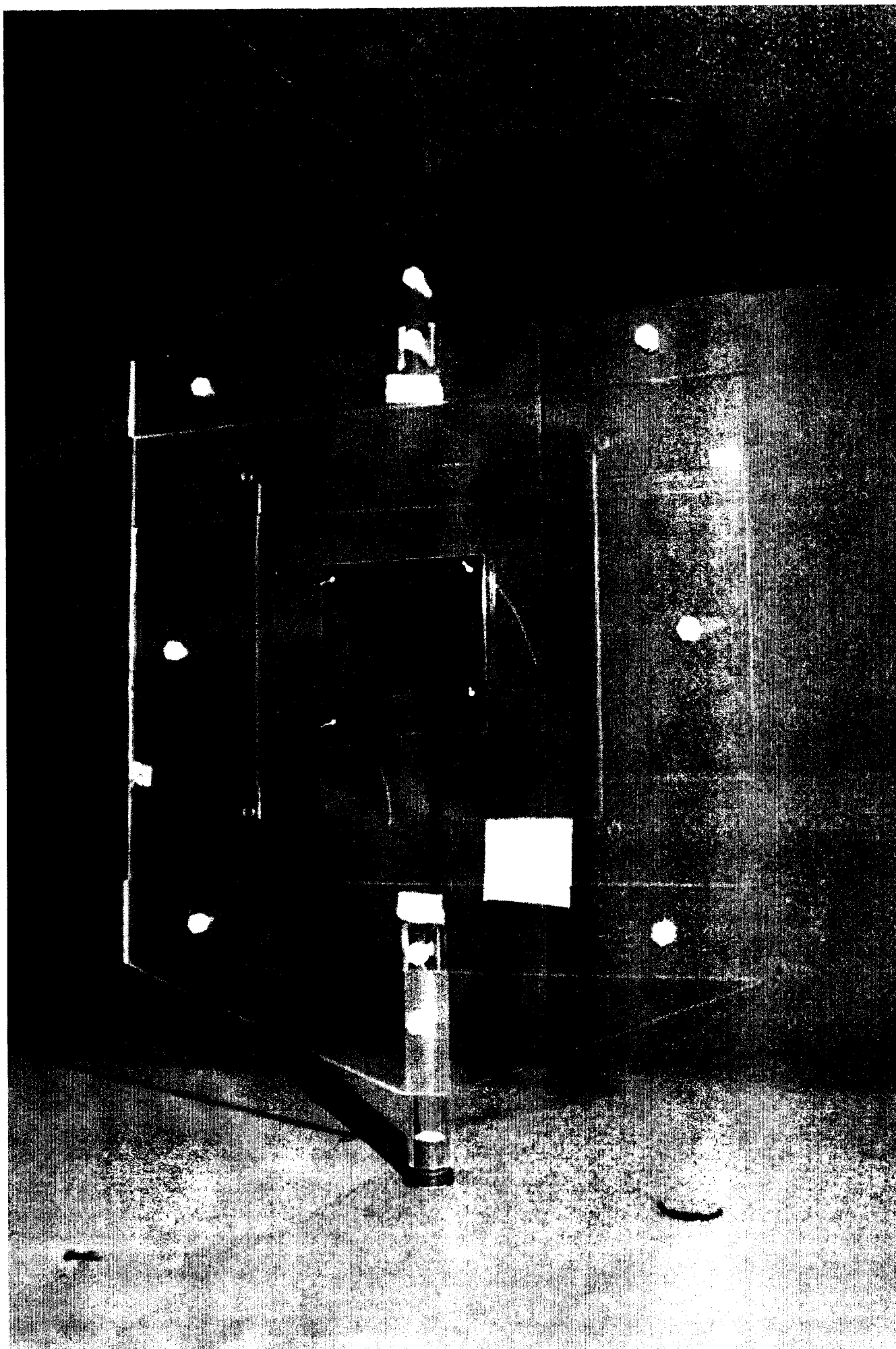
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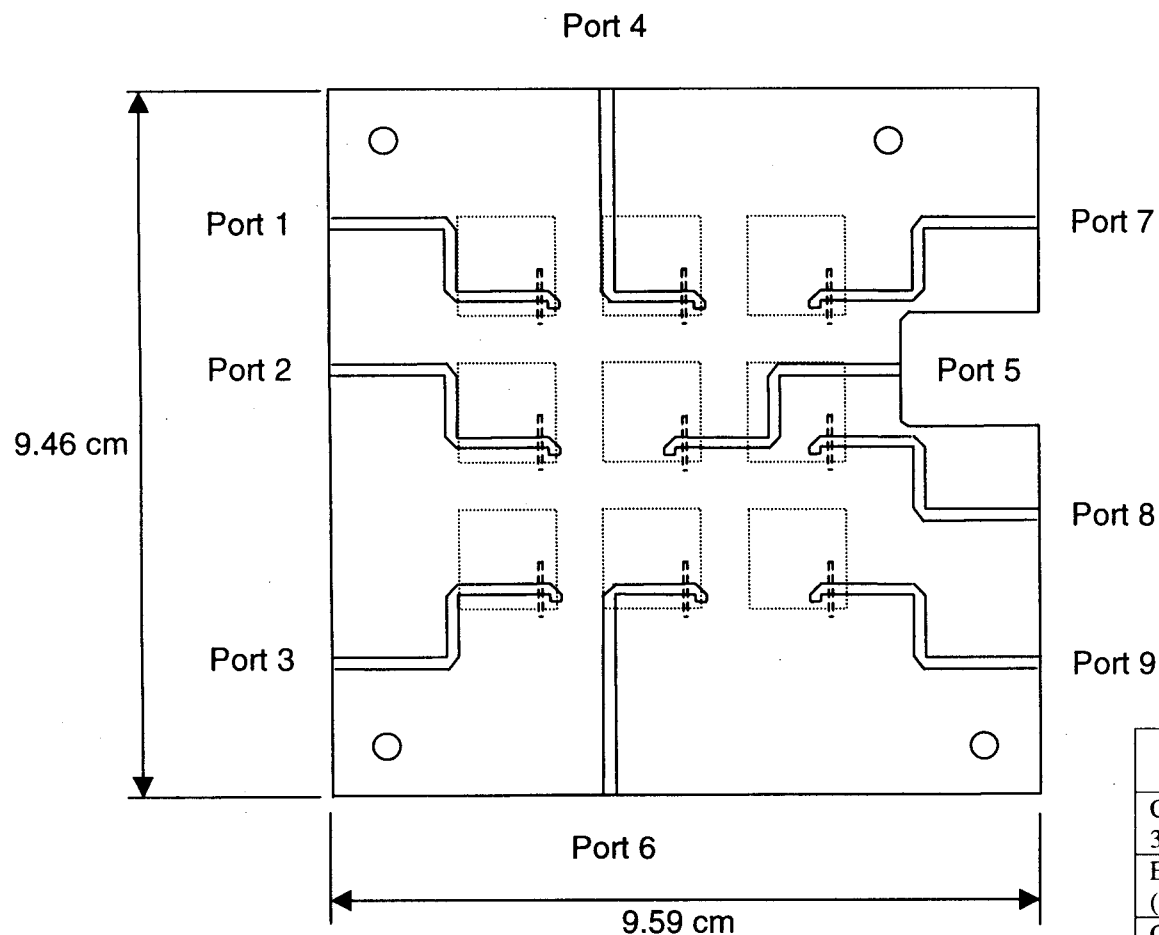
Fig. 11. A view of the measurement chamber showing the rectenna panel holder above the transmit horn.



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Fig. 12. The front side of the 9 element rectenna panel in the measurement chamber.





Note: the reference plane for all ports is the center of the coupling aperture

Port Summary

Port #	Average Eff. Area (cm ²) for H_{pol} and V_{pol}
1	4.57
2	3.43
3	4.36
4	4.07
5	3.81
6	3.73
7	3.99
8	3.03
9	4.15

Panel Summary

	Average Eff. Area (cm ²)	Physical Area (cm ²)
Corner Ports (1, 3, 7 and 9)	4.27	3.87
Edge Center Ports (2, 4 and 6)	3.74	3.87
Center	3.81	3.87
Total array	35.85	34.88

Fig. 13. The definition of ports used to measure the effective area of the panel and the measured effective area at each port.

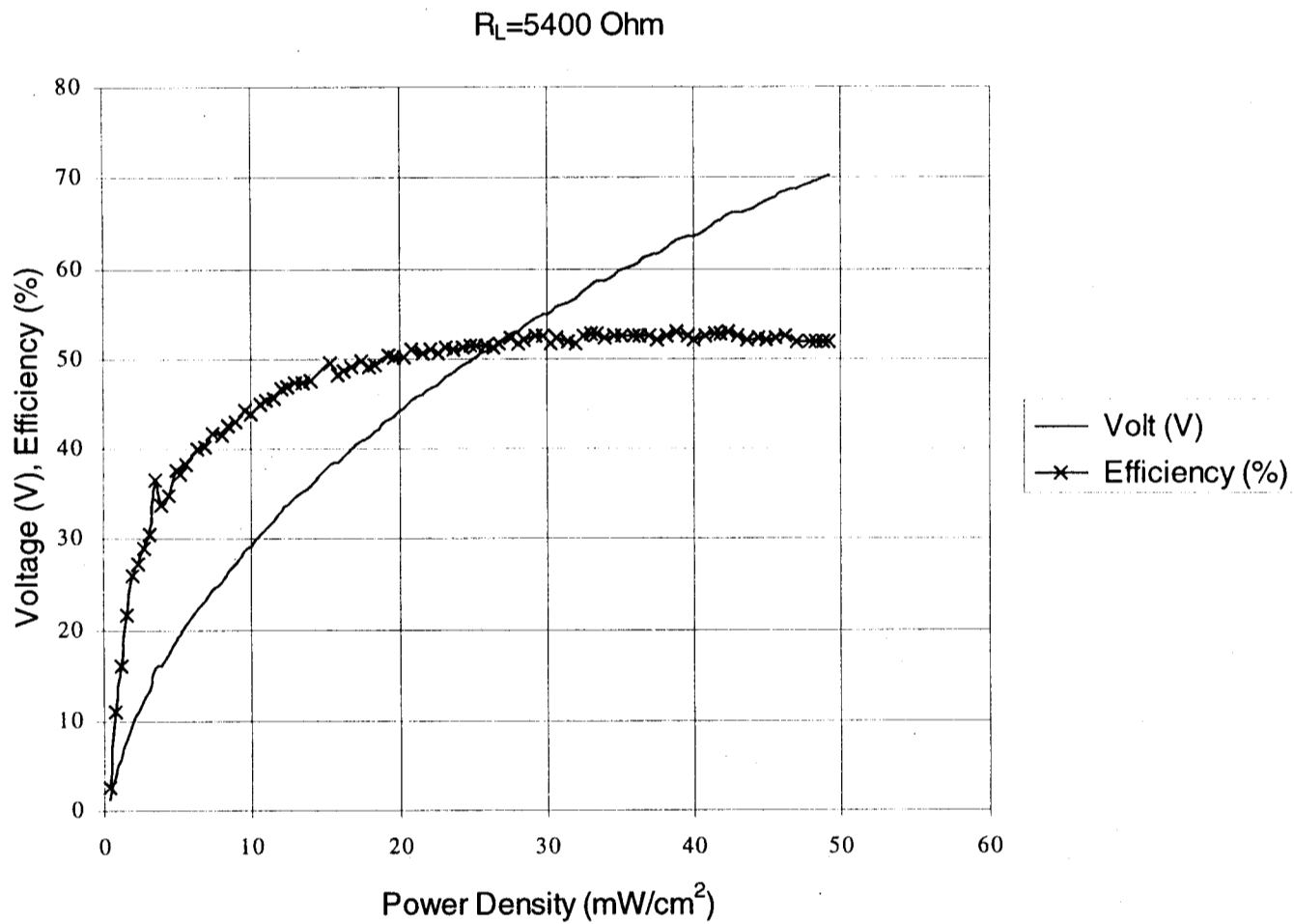


Fig. 15. The output voltage and efficiency for a rectenna panel excited by a Narda 640 standard gain horn. The voltage is the series combination of 18 circuits from two orthogonal polarizations: 9 circuits from H_{pol} and 9 circuits from V_{pol} .

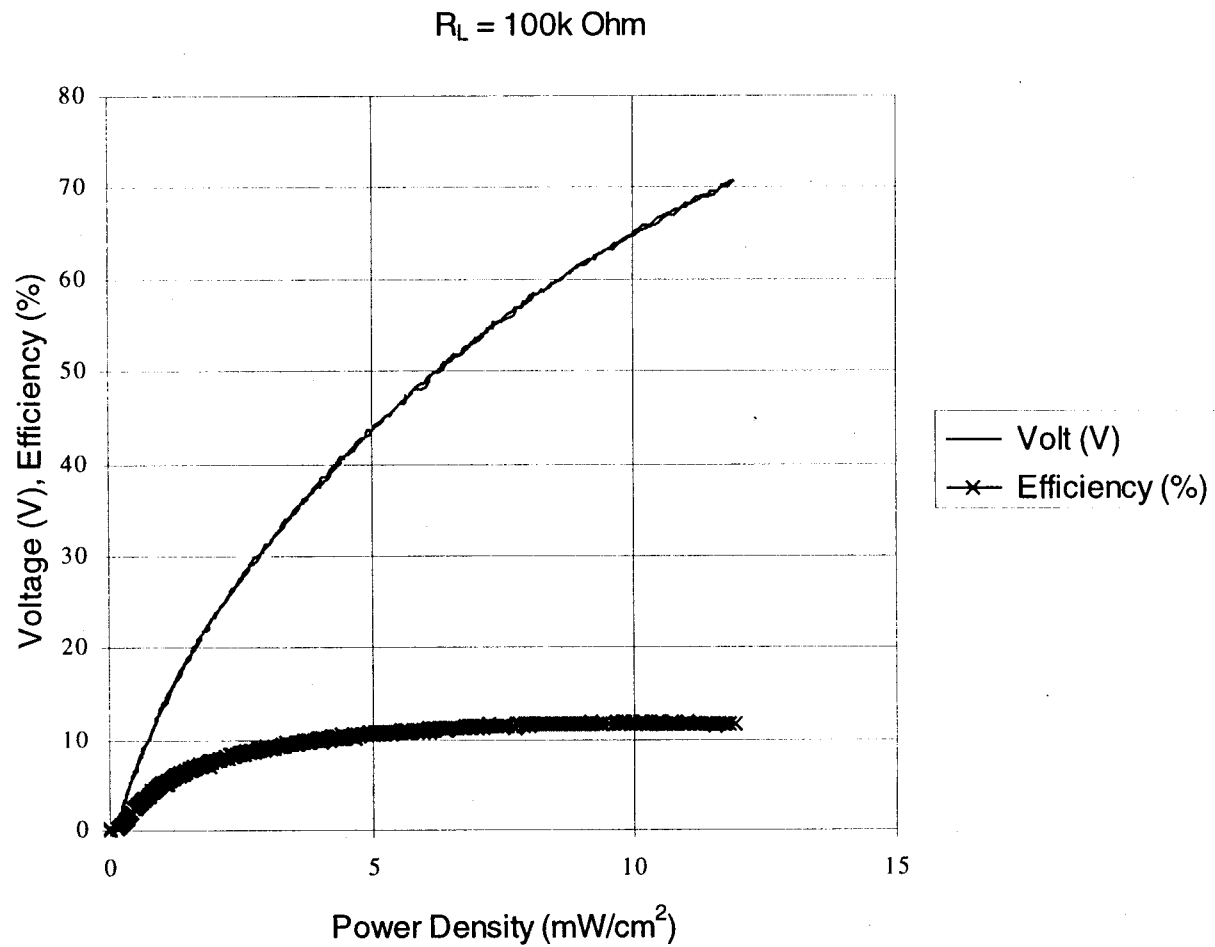


Fig. 16. The output voltage and efficiency for a rectenna panel with load chosen to maximize activator voltage while minimizing the transmit power needed. Note the corresponding drop in efficiency for this application.

Dual-Output Rectenna (LM2577 Boost Regulator Circuit)

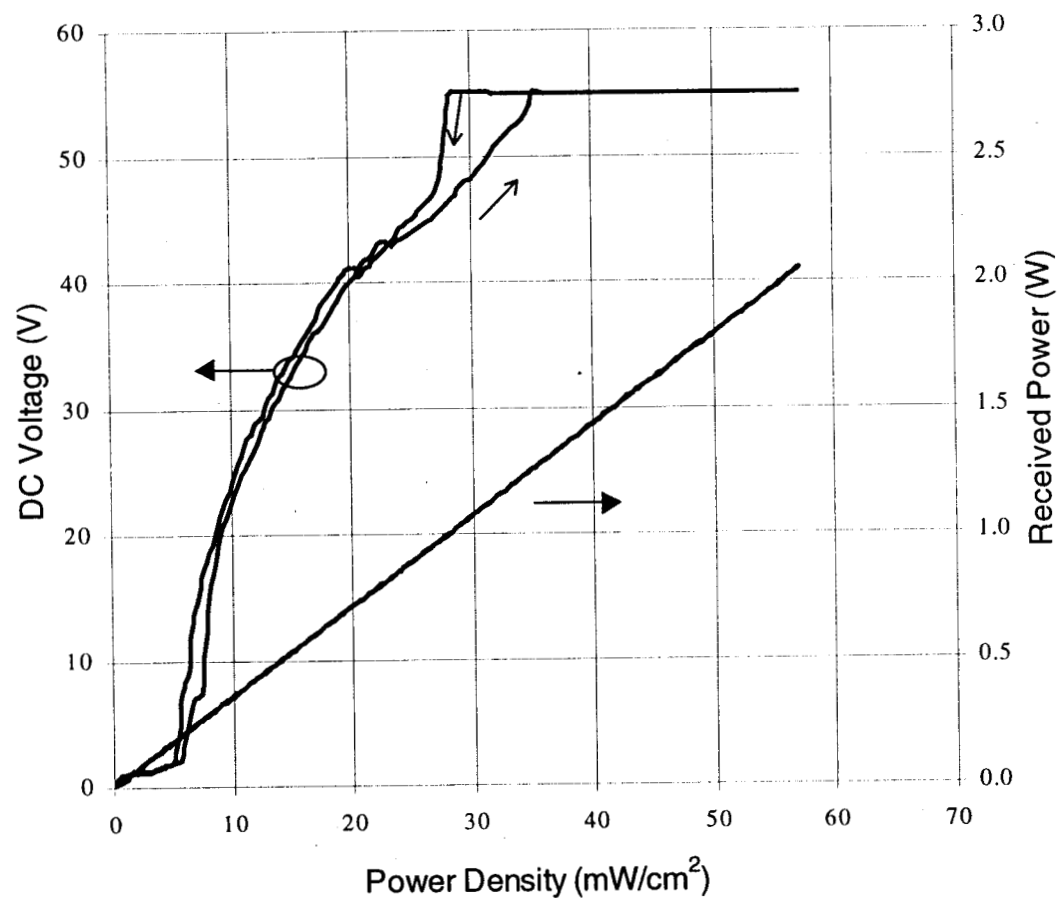


Fig. 17. Representative output voltage of a single rectenna panel using dual boost regulator circuits to provide two DC outputs. 50 V of output voltage can be produced with less than 1.5 W of received power.